REMARKS/ARGUMENTS

The Applicant has carefully considered this application in connection with the Examiner's Action mailed June 16, 2005, and respectfully requests reconsideration of this application in view of the following remarks. The Applicant originally submitted Claims 1-20 in the application. The Applicant previously amended Claims 1, 8 and 15. No amendments are presented in this response. Accordingly, Claims 1-20 are currently pending in the application.

I. Rejection of Claims 1-20 under 35 U.S.C. § 102(b)

The Examiner has rejected Claims 1-20 under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent 5,651,125 to Witt, *et al.* The Applicant respectfully traverses the Examiner's rejection, because Witt does not teach or suggest each and every element of the presently claimed invention. Specifically, with respect to claims 1, 8 and 15, Witt fails to teach or suggest queuing logic, in which instructions and instruction type information are stored in an order based on a priority of the instructions.

Witt is directed in general to microprocessors and, more particularly, to high performance superscalar microprocessors. (Col. 2, lines 51-53.) Witt teaches certain well-known concepts related to microprocessor architecture, including decoding of instructions to generate an opcode, and queuing of the opcode and instruction tags in a reservation station at the input to a functional unit. (See, *e.g.*, column 5, lines 19-40; column 13, lines 22-56.)

The Examiner notes that Witt teaches that the decoder 210 decodes an instruction, thereby generating an opcode that is broadcast to all the functional units. (Column 13, lines 49-51.) In noting this teaching, the Examiner asserts that the instruction opcode taught by Witt is equivalent to an instruction type, as recited in Claim 1. (Examiner's response, § 3.) By drawing this equivalence,

the Examiner thereby implicitly recognizes that the instruction, as provided by the instruction cache 205 to the decoder 210, is a distinct element from the opcode. This distinction is explicitly taught by Witt at column 4, lines 49-59, at which an instruction format is described as including "multiple fields in the following format: OP CODE, OPERAND A, OPERAND B, DESTINATION REGISTER." Thus, an opcode is not an instruction.

However, Claim 1 recites "queuing logic, in which said instructions *and* said instruction type information are stored in an order based on a priority of said instructions." (Emphasis added.) In order for Witt to anticipate this element of Claim 1, Witt must teach the storing of both the instruction, as output by the instruction cache 205, *and* the opcode. However, Witt only teaches storing the opcode. In the very passage of Witt relied upon by the Examiner to anticipate this element, Witt teaches that the instruction is not stored after it is decoded. Specifically, Witt states at column 13, line 49-51, "[w]hen a particular instruction is decoded by decoder 210, decoder 210 sends the OP CODE of the decoded instruction to the appropriate functional unit ...." Continuing at column 14, lines 6-11, Witt states:

> With respect to the ADD opcode in the present example, one of the functional units, namely the arithmetic logic unit (ALU) in integer core 215 will recognize the opcode type and latch in its reservation station 220 the information including opcode, A operand tag, A operand (if available), B operand tag, B operand (if available) and destination tag.

These passages only teach storing of the opcode by queuing logic. There is no express or inherent teaching in these passages cited by the Examiner, nor in any passage the Applicant can identify, of queuing logic, in which the instruction *and* opcode are stored in an order based on a priority of the instructions, as recited in Claim 1.

A claim is only anticipated "if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." M.P.E.P. § 2131. Because Witt fails to expressly or inherently describe queuing logic that stores *both* instructions and instruction type information, Witt fails to anticipate each and every element of Claim 1, and is not a valid anticipatory reference. Furthermore, under the same reasoning, Witt does not anticipate of independent Claims 8 and 15. Therefore, Claims 1, 8 and 15, and those claims depending therefrom, are allowable.

Accordingly, the Applicant respectfully requests that the Examiner withdraw the rejection under 35 U.S.C §102(b) and allow issuance of Claims 1-20.

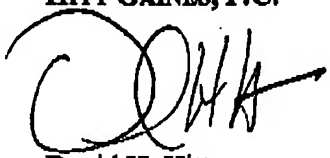
II. Conclusion

In view of the foregoing amendments and remarks, the Applicant now sees all of the claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-20.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

HITT GAINES, P.C.



David H. Hitt
Registration No. 33,182

Dated: August 25, 2005

P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800